REMARKS

Claims 1-17 are pending in this application, all of which stand rejected. It is submitted that all the claims are patentable for the reasons set forth below.

Objection to the Title

The title of the invention has been amended in response to the Examiner's objection (see paragraph 3 of the Office Action). Withdrawal of the objection to the title is respectfully solicited.

Claims 1-17 have been rejected under 35 U.S.C. §102(b) as being anticipated by Itoh et al.

In the statement of the rejection, the Examiner asserted that Itoh et al. discloses a semiconductor device capable of operating stably with reduced power consumption identically corresponding to what is claimed. This rejection is respectfully traversed.

It is well established precedent that the factual determination of lack of novelty under 35 U.S.C. §102 requires the identical disclosure in a single reference of each element of the claimed invention, such that the identically claimed invention is placed into the possession of one having ordinary skill in the art. *See EMI Group N. Am., Inc. v. Cypress Semiconductor Corp.*, 268 F.3d 1342, 60 USPQ2d 1423 (Fed. Cir. 2001); *Helifix Ltd. v. Blok-Lok, Ltd.*, 208 F. 3d 1339, 54 USPQ2d 1299 (Fed. Cir. 2000); *Electro Medical Systems S.A. v. Cooper Life Sciences, Inc.*, 34 F.3d 1048, 32 USPQ2d 1017 (Fed. Cir. 1994).

Applicants submit that Itoh et al. does not disclose, among other things, changing a back gate potential of at least the first conductivity type transistor in data wiring from that in data

reading in response to an address signal and an operation mode designating signal, as recited in independent claim 1.

Itoh et al. describes reducing power dissipation without impairing high speed operationability. A power source is constructed into a hierarchical structure having a main power supply and a sub power supply. A MOS transistor with a low threshold voltage has a back gate voltage controlled in accordance with an operation mode. Thus, a threshold voltage of the MOS transistor is controlled to be low in absolute value in an active cycle for high speed operation, and to be high in absolute value in a standby cycle for reduced leakage current. Itoh does not disclose changing the threshold voltage between a data writing mode and a data read mode.

In an SRAM array of Ito et al., a well voltage or a back gate voltage is set constant, or to a power supply voltage and a ground voltage for a PMOS transistor and an NMOS transistor, respectively. This prevents an increase in current consumption due to charging and discharging of well capacitance upon changing of the well voltage. The power supply voltage to an SRAM is set as high as 3.3V, and the threshold voltage of an SRAM transistor is made high in absolute value. The high power supply voltage of 3.3V is used for ensuring the high speed operation performance of SRAM transistors.

In Itoh et al., the substance voltage of an SRAM array is kept constant, and is not changed in accordance with an operation mode. In addition, DRAM array has the substrate voltage set at a constant, negative voltage.

Applicants submit that the Examiner merely refers to the hierarchical structure of a CMOS inverter in a logic circuit and an interface circuit of an integrated circuit of Itoh et al., but did not consider the description on the SRAM array in Itoh et al., as discussed above. Itoh et al.

does not disclose controlling the back gate voltage according to an operation mode as recited in independent claim 1. Accordingly, Itoh does not identically disclose a semiconductor memory device including all the limitations recited in independent claim 1. Dependent claims 2-17 are also patentably distinguishable over Itoh et al. at least because they include all the limitations recited in independent claim 1, respectively. Applicants, therefore, submit that the imposed rejection of claims 1-17 under 35 U.S.C. §102(b) for lack of novelty as evidenced by Itoh et al. is not factually viable and, hence, respectfully solicit withdrawal thereof.

Conclusion

It should, therefore, be apparent that the imposed rejections have been overcome and that all pending claims are in condition for immediate allowance. Favorable consideration is, therefore, respectfully solicited.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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